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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,847	09/24/2003	Timothy A. Rost	TI-35258	4436

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EXAMINER	
HA, NGUYEN T	

ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 05/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	10/669,847	ROST ET AL.	
	Examiner	Art Unit	
	Nguyen T Ha	2831	

-- The MAILING DATE of this communicati n appears on the cover sheet with the corresp nd nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) *12-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 43-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Claims 1-11 and 43-53 filed on 4/23/2004 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-11 and 43-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Block et al. (US 6,737,728) in view of Doan et al. (US 6,303,953).

Regarding claim 1, Block et al. disclose a capacitor for integrated circuit (figure 2) comprising:

- a bottom electrode (104), said bottom electrode positioned over a top metal level and coupled to a first interconnect (101) of the top metal level;
- a capacitor dielectric (105) coupled to the bottom electrode;
- a top electrode (106) coupled to the capacitor dielectric; and the top electrode (106) is coupled to a second interconnect (102) of the top metal level.

Block et al. lack:

sidewalls positioned at a perimeter of the top metal level capacitor, the sidewalls coupled to the top metal level, the bottom electrode, the capacitor dielectric, and a portion of the top electrode.

Doan et al. teach:

sidewalls (112) positioned at a perimeter of the top metal level capacitor, the sidewalls coupled to the top metal level, the bottom electrode, the capacitor dielectric, and a portion of the top electrode (figure 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modified the Block et al's capacitor to have a sidewalls as taught by Doan in order to provide an improve structure for fabrication of high value capacitor.

Regarding claims 2 & 3, Block et al. disclose the dielectric comprising of a high-k material comprising TaOx (column 6, lines 3-4).

Regarding claims 4 & 5, Block et al. disclose the bottom electrode and top electrode comprising of a layer of TaN and a layer of TiN (column 5, lines 56-57 and column 7, lines 8-10).

Regarding claim 6, the teaching of Doan et al. further included the sidewalls being comprised of SiN (column 5, lines 56-57).

Regarding claim 7, Block et al. disclose the first interconnected and the second interconnected comprised of Cu (column 4, lines 46-47).

Regarding claim 8, Block et al. disclose the first interconnected (101) being coupled to a power supply rail (figure 2).

Regarding claim 9, Block et al. disclose the second interconnect (102) being coupled to GND (figure 2).

Regarding claim 10, Block et al. disclose the top metal level capacitor is a decoupling capacitor from a supply voltage to ground (figure 2).

Regarding claim 11, Block et al. disclose a top metal level capacitor for integrated circuits (figure 2) comprising:

- a bottom electrode (104) comprised of a layer of TaN and a layer of TiN (column 5, lines 56-57), the bottom electrode positioned over a top metal level and coupled to a first interconnect (101) of the top metal level;
- a capacitor dielectric (105) comprised of TaOx (column 6, lines 3-4) coupled to the bottom electrode;
- a top electrode (106) comprised of a layer of TiN and a layer of TaN (column 7, lines 8-10) coupled to the capacitor dielectric; and
- wherein the layer of TaN of the top electrode (column 7, lines 8-10) being coupled to a second interconnect (102) of the top metal level, the first interconnect is coupled to a supply voltage and is comprised copper

(column 4, lines 46-47), and the second interconnect is coupled to ground and is comprised of copper (figure 2).

Block et al. lack:

sidewalls comprised of SiN positioned at a perimeter of the top metal level capacitor, and sidewalls coupled to the top metal level, the bottom electrode, the capacitor dielectric and a portion of the top electrode.

Doan et al. teach:

sidewalls comprised of SiN (column 5, lines 56-57) positioned at a perimeter of the top metal level capacitor, and sidewalls coupled to the top metal level, the bottom electrode, the capacitor dielectric and a portion of the top electrode (figure 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modified the Block capacitor as taught by Doan to have the sidewall being formed from silicon nitride in order to provide an improve structure for fabrication of high value capacitor.

Regarding claim 43, Block et al. disclose a capacitor for integrated circuits (figure 2) comprising:

- a bottom electrode (104) positioned over a top metal level and coupled to a first interconnect (101) of the top metal level;
- a capacitor dielectric (105) coupled to the bottom electrode;
- a top electrode (106) coupled to the capacitor dielectric and to a second interconnect of the top metal level.

Block t al. lack:

- sidewalls positioned at a perimeter of the top metal level capacitor, said sidewalls coupled to the top metal level, the bottom electrode and the capacitor dielectric.

Doan et al. teach

sidewalls (112) positioned at a perimeter of the top metal level capacitor, the sidewalls coupled to the top metal level, the bottom electrode, the capacitor dielectric, and a portion of the top electrode (figure 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modified the Block et al's capacitor to have a sidewalls as taught by Doan in order to provide an improve structure for fabrication of high value capacitor.

Regarding claims 44 & 45, Block et al. disclose the dielectric comprising of a high-k material comprising TaOx (column 6, lines 3-4).

Regarding claims 46 & 47, Block et al. disclose the bottom electrode and top electrode comprising of a layer of TaN and a layer of TiN (column 5, lines 56-57 and column 7, lines 8-10).

Regarding claim 48, the teaching of Doan et al. further included the sidewalls being comprised of SiN (column 5, lines 56-57).

Regarding claim 49, Block et al. disclose the first interconnected and the second interconnected comprised of Cu (column 4, lines 46-47).

Regarding claim 50, Block et al. disclose the first interconnected (101) being coupled to a power supply rail (figure 2).

Regarding claim 51, Block et al. disclose the second interconnect (102) being coupled to GND (figure 2).

Regarding claim 52, Block et al. disclose the top metal level capacitor is a decoupling capacitor from a supply voltage to ground (figure 2).

Citation Relevant of Prior Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Andricacos et al. disclose compound electrode stack capacitor.

b. Ymamichi et al. disclose highly integrated thin film capacitor with high dielectric constant layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen T Ha whose telephone number is 571-272-1974. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nguyen T. Ha
May 20, 2004

Dean A. Reichard 5/21/04
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